REMARKS

At the outset, Applicants thank the Examiner for the courtesies extended to Applicants' representatives in a personal interview on July 30, 2004 and for the thorough review and consideration of the subject application. The final Office Action of April 6, 2004 has been received and its contents carefully reviewed.

Claims 1, 8, 13, 18, and 20 are hereby amended and claims 22-32 are hereby added. Accordingly, claims 1-32 are currently pending. Applicant respectfully submits that claims 22-32 have been added to reflect subject matter discussed in the interview conducted on July 30, 2004. Reexamination and reconsideration of the pending claims is respectfully requested.

In the Final Office Action, the Examiner rejected claims 1, 2, 4, 6, 8, 9, 11, 20, and 21 under 35 U.S.C. § 102(e) as being anticipated by Shin (U.S. Patent No. 6,323,836); rejected claims 3, 5, 7, 10, and 12 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Nakano et al. (U.S. Patent No. 6,229,513); and rejected claims 13-19 under 35 U.S.C. § 103(a) as being unpatentable over Nakano et al. in view of the Related Art shown in Figure 3. The rejections of these claims are traversed and reconsideration of the claims is respectfully requested in view of the following remarks.

The rejection of claims 1, 2, 4, 6, 8, 9, 11, 20, and 21 under 35 U.S.C. § 102(e) as being anticipated by Shin is traversed and reconsideration is respectfully requested.

Independent claim 1 is patentable over Shin in that claim 1 recites a combination of elements including, for example, "a timing controller... for receiving a data clock inputted from the exterior thereof to alternately output the data from the plurality of groups of said line memory to the driving circuit every period of the data clock...." Shin fails to teach, either expressly or inherently, at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claims 2, 4, and 6, which depend from claim 1, are also patentable over Shin.

Independent claim 8 is patentable over Shin in that claim 8 recites a combination of elements including, for example, "a timing controller... for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the data clock... and for alternately outputting the data in each of the groups to the driving circuit during each period of the input data clock." Shin fails to teach, either expressly or inherently, at least this feature of

the claimed invention. Accordingly, Applicant respectfully submits that claims 9 and 11, which depend from claim 8, are also patentable over Shin.

Independent claim 20 is patentable over Shin in that claim 20 recites a combination of elements including, for example, "a data clock generating step of frequency-dividing an input first data clock at a frequency-division ratio... to generate a second data clock; a data outputting step of alternately outputting a desired data unit from each of said groups at a different time during one period of the second data clock...." Shin fails to teach, either expressly or inherently, at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claim 21, which depends from claim 20, is also patentable over Shin.

The rejection of claims 3, 5, 7, 10, and 12 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Nakano et al. is traversed and reconsideration is respectfully requested.

Applicants respectfully submit that claims 3, 5, 7, 10, and 12 are patentable at least because these claims depend from independent claims 1 and 8, which are believed to be patentable over the cited references.

The rejection of claims 13-19 under 35 U.S.C. § 103(a) as being unpatentable over Nakano et al. in view of the Related Art shown in Figure 3 is traversed and reconsideration is respectfully requested.

Independent claim 13 is patentable over Nakano et al. in view of the Related Art shown in Figure 3 in that claim 13 recites a combination of elements including, for example, "a timing controller... connected to the line memory and the driving circuit, for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the input data clock... and for alternately outputting the two pixel data in each of the groups to the driving circuit during each period of the input data clock." Neither Nakano et al. nor the Related Art shown in Figure 3, singly or in combination, teach or suggest at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claims 14-17, which depend from claim 13, are also patentable over Nakano et al. in view of the Related Art shown in Figure 3.

Claim 14 depends from independent claim 13 and, therefore, includes at least the aforementioned combination of elements set forth in claim 13. As described above Nakano et al. fails to teach at least the aforementioned combination of claimed elements. The Related Art

shown in Figure 3 was cited as allegedly disclosing the various elements of claim 14. Without reaching the merits of this assertion, Applicant respectfully submits the Related Art shown in Figure 3 fails to cure the aforementioned deficiency of Nakano et al. Accordingly, the Applicant respectfully submits that claim 14 is patentable over Nakano et al. in view of the Related Art shown in Figure 3.

Independent claim 18 is patentable over Nakano et al. in view of the Related Art shown in Figure 3 in that claim 18 recites a combination of elements including, for example, "a timing controller... connected to the latch circuit and the driving circuit, for receiving a data clock inputted from the exterior thereof to alternately output each one pixel data to the driving circuit at a desired time interval during one period of the data clock." Neither Nakano et al. nor the Related Art shown in Figure 3, singly or in combination, teach or suggest at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claim 19, which depends from claim 18, is also patentable over Nakano et al. in view of the Related Art shown in Figure 3.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: October 4, 2004

Respectfully submitted,

By Reg. No. 41788
Kurt M. Eaton
Registration No.: 51,640
MCKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorney for Applicant

DC:50286858.1